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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,712	03/11/2002	Hiroshi Takatori	PW 024 9733 P12825	3533

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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,712	TAKATORI ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *327,627*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. In claims 1,6,11 and 19, lines 4-5,4-5,8-9 and 7-8 recite "estimating an error (or error estimator module) ... as a corrected value". It appears that the estimating step has a contradicting limitation. How can an estimating an error

step become a "corrected value"? In other words, how can an error become a correct value? Thus, the claim is vague and indefinite.

b. In claims 1,6,11 and 19 lines 9-10, recite "correcting the tentative value to the corrected value...".In the specification, p.7, lines 18-19, describes that "... the command to select the corrected value, rather than the tentative value.". However, according to the claim, it appears that the tentative value, calculated by Decision Circuit (32 in Fig.4) is corrected to the corrected value. Does this mean that the Decision Circuit holds the corrected value after the "correcting step"?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6,8-10 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riggle US 2001/0016926 A1 in view of Powell, II et al. USP 6,084,931 (Powell).

Regarding claims 1,6 and 19, Riggle teaches a method and apparatus of a decision system in high-speed data transmission, comprising: a data decision circuit (16) to determine a value of an input signal at a decision instance and to

hold the value as a tentative value; an error estimator module (15,56) to determine an error value, to amplify the error value, and to hold the amplified error value as a corrected value (note paragraph 41 wherein the inverter has the opposite bit from the bit output from data decision circuit, 16); an error correction module (57,58) to determine whether the tentative value should be overridden by the corrected value (note paragraph 41, lines 28-37). And although Riggle does not explicitly teach an error verifier module to determine whether the amplified error value is within a marginal range, it is inherent that the inverter (56) includes such function as the output of inverter is selected and output by the MUX (58) when the value is within the marginal range (note paragraph 42, the marginal range having a logical ones or zeros).

However, Riggle does not explicitly teach a transition detecting module to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period.

Powell teaches the transition detecting module (200 in Fig.1) to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Powell in the system of Riggle for the purpose of detecting the symbol center, thus improve synchronization (note col.2, lines 35-37).

Regarding claims 2-5,8-10,20 and 21, Riggle in view of Powell teach all subject matter claimed, as applied to claim 1,6 or 19. Powell further teaches wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the input signal is in transition (note col.3, lines 4-14 having three sampling times), one-half a symbol period before and after the decision instance, s(t).

And Powell further teaches the transition detecting module (200 in Fig.1 further illustrated in Fig.8) including an adder (246,248) to add the adjacent sample values, an absolute value circuit (224, note col.6, lines 29-31) to make positive the added adjacent sample values, and a comparator (226,228,230) to compare the added adjacent sample values to a reference value (1XDEV,2XDEV,3XDEV).

4. Claims 11-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riggle US 2001/0016926 A1 in view of Powell, II et al. USP 6,084,931 (Powell) and Moriuchi USP 6,556,637 B1 (Moriuchi).

Regarding claim 11 and 14, Riggle teaches a method and apparatus of a decision system in high-speed data transmission, comprising: a data decision circuit (16) to determine a value of an input signal at a decision instance and to hold the value as a tentative value; an error estimator module (15,56) to determine an error value, to amplify the error value, and to hold the amplified error value as a corrected value (note paragraph 41 wherein the inverter has the opposite bit from the bit output from data decision circuit, 16); an error correction

module (57,58) to determine whether the tentative value should be overridden by the corrected value (note paragraph 41, lines 28-37). And although Riggle does not explicitly teach an error verifier module to determine whether the amplified error value is within a marginal range, it is inherent that the inverter (56) includes such function as the output of inverter is selected and output by the MUX (58) when the value is within the marginal range (note paragraph 42, the marginal range having a logical ones or zeros).

However, Riggle does not explicitly teach a transition detecting module to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period.

Powell teaches the transition detecting module (200 in Fig.1) to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Powell in the system of Riggle for the purpose of detecting the symbol center, thus improve synchronization (note col.2, lines 35-37).

However, Riggle in view of Powell do not explicitly teach an analog-to-digital converter, a phase detector, a loop filter and an oscillator.

Moriuchi teaches (see Fig.4) an analog-to-digital converter (33), a phase detector (61), a loop filter (62) and an oscillator (64) to output a sampling clock for the analog-to-digital converter. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Moriuchi in the

system of Riggle in view of Powell for the purpose of having a timing recovery PLL circuit providing a stable clock, as taught by Moriuchi (note col.7, lines 25-33).

Regarding claims 12,13 and 16, Riggle in view of Powell and Moriuchi teach all subject matter claimed, as applied to claim 11. Powell further teaches wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the input signal is in transition (note col.3, lines 4-14 having three sampling times), one-half a symbol period before and after the decision instance, s(t).

And Powell further teaches the transition detecting module (200 in Fig.1 further illustrated in Fig.8) including an adder (246,248) to add the adjacent sample values, an absolute value circuit (224, note col.6, lines 29-31) to make positive the added adjacent sample values, and a comparator (226,228,230) to compare the added adjacent sample values to a reference value (1XDEV,2XDEV,3XDEV).

5. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riggle US 2001/0016926 A1 in view of Powell, II et al. USP 6,084,931 (Powell) and Moriuchi USP 6,556,637 B1 (Moriuchi).and in further view of Shenoi USP 6,549,604 B2.

Regarding claims 17 and 18, Riggle in view of Powell and Moriuchi teach all subject matter claimed, as applied to claim 11. However, Riggle in view of Powell

and Moriuchi do not explicitly teach wherein the input signal is received from a T1 data transmission system including a plurality of cascaded T1 links.

Shenoi teaches a receiver (see Fig.3) receiving a T1 signal (T1-SIG) and providing a clock recovery and detection of phase transients, wherein cascaded T1 links are well-known in the art for a T1 systems. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Shenoi in the system of Riggle in view of Powell and Moriuchi of receiving a T1 signal and providing the clock recovery for the purpose of increasing the flexibility of the system by performing clock recovery to various types of signals including T1 signals.

Allowable Subject Matter

6. Claims 7 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
7. The following is a statement of reasons for the indication of allowable subject matter: Present application discloses a decision system in a high-speed data transmission comprising a data decision circuit, error estimator module, error verifier module, transition detecting module and an error correction module as configured in figure 5. Prior art does not teach the error verifier module configured to include an absolute

value circuit and a comparator as illustrated in the fifth figure to make the error value a positive number and to compare the error value to a reference value.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kaku et al. USP 5,719,907 teach a selector selecting either a corrected value or tentative value.

Jungerman, USP 6,629,272 B1 teaches an error performance analyzer displaying transition of an input signal switching from high and low levels.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
8/4/05

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PRIMARY EXAMINER